Introducing a Family of eGaN® FETs for Multi-Megahertz Hard Switching Applications

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The ultra high speed switching capabilities of gallium nitride transistors are taken to the next level with the EPC8000 series featuring switching transition speeds in the sub nano-second range. These devices are capable of hard switching applications above 10 MHz. Figure 1 shows a photo image of the new EPC8000 device mounting (bump) side.

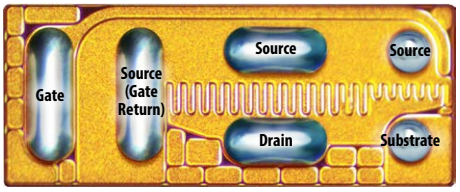

Figure 1: Mounting side of EPC8000 series eGaN FET

In this application note we present the EPC8000 series devices and highlight some of the key features that make this transistor family suitable for high frequency applications. That will be followed by two application examples, a 10 MHz envelope tracking converter and a 6.78 MHz class D wireless power transfer system. In conclusion, small signal RF characteristics will also be provided.

EPC8000 Device Family Overview

Table 1 lists the EPC8000 family of devices and highlights the various key characteristics. These transistors are available in $R_{DS(on)}$ values from 125 mΩ through 530 mΩ, and three blocking voltage capabilities, 40 V, 65 V and 100 V. Building on EPC's industry leading enhancement mode GaN technology, the EPC8000 family of devices has been designed with additional features that make them easy to use in high frequency applications. Next is a summary of the most prominent key features:

1. **Separate gate return (source)** – The separate gate return (source) for the gate circuit limits the common source inductance to inside the device itself. This reduction in common source inductance is critical to high frequency performance. The efficiency impact of the common source reduction is well documented [1, 2], and designers can thus focus more of their attention on reducing the loop inductance [2].
2. **Low inductance gate –** The wider solder bar for the gate circuit significantly reduces the inductance of the gate circuit, thereby enhancing the speed of the connection to the gate driver.
3. **High dv/dt immunity** – An important metric for dv/dt immunity is the Miller ratio, which is an indicator of how susceptible gates are to turning back on at high dv/dt. For the ultra-fast EPC8000 family of devices the Miller ratio (Q_{GD}/Q_{GS1}) has been reduced to below 0.38, well below the industry standard of 1.
4. **Orthogonal gate and drain circuit layout** – The gate and drain solder bars are designed so that optimal current paths are 90° with respect to each other. This significantly reduces the interaction of the gate circuit current with the drain circuit current, and effectively reduces the common source inductance (CSI) of the device.
5. **Low internal parasitic inductances** – The internal routing has been designed with high frequency applications in mind, and therefore internal parasitic inductances have been minimized for both the drain and gate circuits.
6. **Reduced Q_{GD}** – The EPC 8000 family is targeted for lower current applications, and to maximize performance the Miller charge has been reduced, improving switching performance by decreasing the voltage transition times. This comes at a slight increase in Q_{GS2} and di/dt losses, but overall total switching losses are still closely matched (see Figure 2 for details).

The EPC8000 family of devices has been designed to target low power, compact, high frequency applications.

Part Number	BV_{DSS} (V)	$R_{DS(on)}$ Max (mΩ) (V_{GS} = 5 V, I_D = 0.5 A)	Peak I_D Min (A) (Pulsed, 25°C, T_{pulse} = 300 µs)	Typical Charge (pC)					Typical Capacitance (pF) (V_{DS} = BV/2, V_{GS} = 0 V)		
				Q_G	Q_{GD}	Q_{GS}	Q_{OSS}	Q_{RR}	C_{ISS}	C_{OSS}	C_{RSS}
EPC8004	40	125	7.5	358	31	110	493	0	45	17	0.4
EPC8009	65	138	7.5	380	36	116	769	0	47	17	0.4
EPC8002	65	530	2	141	9.4	59	244	0	21	5.9	0.1
EPC8010	100	160	7.5	354	32	109	1509	0	47	18	0.2

Table 1. *Table data subject to change. Please refer to the Product section on www.epc-co.com.*

Designing with the EPC8000

In this section some simple design procedures are provided to help designers take full advantage of the EPC8000 series devices' superior electrical characteristics.

Figure 3 shows a schematic representation of the new EPC8000 device detailing the return path for

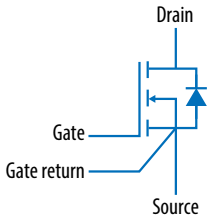

Figure 3: Schematic symbol for the EPC8000 family of devices.

the gate. Even though this pad is connected to the source internally in the device, it should be regarded as floating and should ONLY be connected to the gate driver ground, which in turn is NOT connected to the circuit ground, as shown in Figure 4 (left). High dv/dt and di/dt mean that a large voltage (~10 V) can appear during switching transients across this node with respect to ground, correctly creating a ground bounce condition for the gate driver. Figure 4 (right) shows how to correctly apply the gate return when using the LM5113 half bridge gate driver for both the high and low side FETs. Alternatively, the gate driver supply can be completely isolated from the main supply power.

The ground bounce issue will now affect the signal driving the gate driver instead of the gate itself, and similar precautions need to be taken to prevent false gate triggering. Figure 5 shows that by adding a small capacitance across the input of the gate driver and its local ground, and supplying the signal through a small resistor, the effect of ground bounce can be reduced. The gate driver input has hysteresis and will be able to overcome the remainder of the ground bounce voltage and prevent false triggering.

The EPC8000 series FETs has a new footprint as shown in Figure 6. The recommended PCB layout and stencil information are provided in the datasheet, which is available at www.epc-co.com.

In all other respects, the EPC8000 series FETs can be treated in much the same manner as any of the earlier generation eGaN FETs.

Next is an example of a power stage for an envelope tracking converter using a 65 V EPC8000 series device and a voltage mode class D wireless power transfer system using the EPC8004.

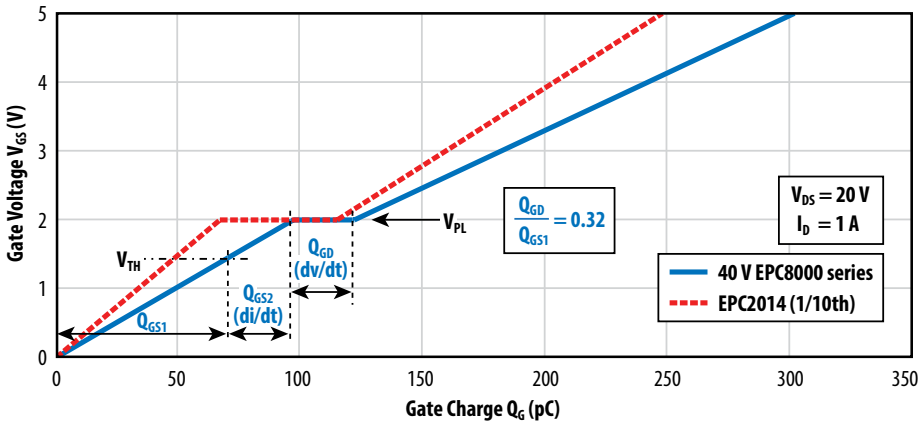

Figure 2: Gate charge comparison of EPC8000 series vs EPC2014

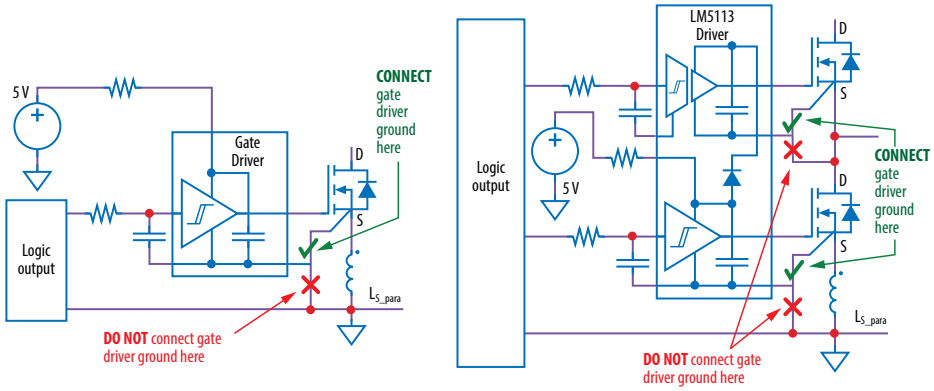

Figure 4: Correct gate driver ground connection when using the EPC8000 series FETs

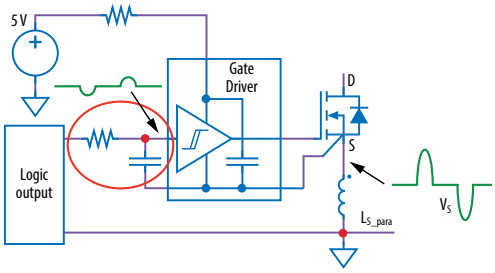

Figure 5: Recommended method to reduce impact of ground bounce on the gate driver signal

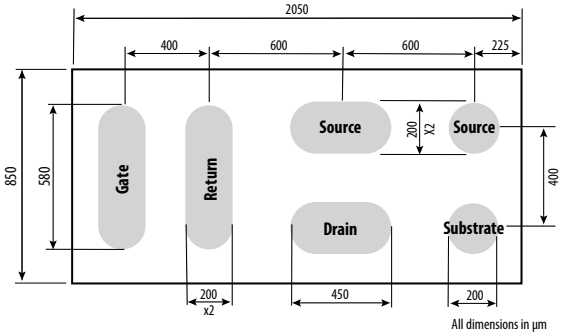

Figure 6: EPC8000 series FET footprint (solder bump view)

Design Example: 10 MHz Envelope Tracking Converter

In the first example, a 65 V EPC8000 series device will be demonstrated in a 42 V to 20 V, 40 W buck converter operating at 10 MHz. The basic power circuit is shown in Figure 7 where L_{Buck} = 2.2 µH (IHLP1616BZ01) and C_{out} = 2 x 4.7 µF (CGA4J3X5R1V475M125AB). The main supply (V_{DD}) bus caps were 100 nF (C1005X5R1H104K050BB). The board was designed using the optimal layout technique [2] to ensure the highest efficiency. The choice of low inductance supply bus capacitors is also critical even when using the optimal layout.

Figure 8 shows a photo of the EPC9025 evaluation board fitted with EPC8000 devices and the LM5113 gate driver IC. The right image shows the details of the power circuit with the gate driver IC. To maintain low inductance in the gate circuit, two parallel connected size 0201 resistors were used side by side for the gate resistors, as well as keeping the gate driver IC very close to the devices. It should be noted that the area occupied by the converter is smaller than the footprint of a SO-8 package.

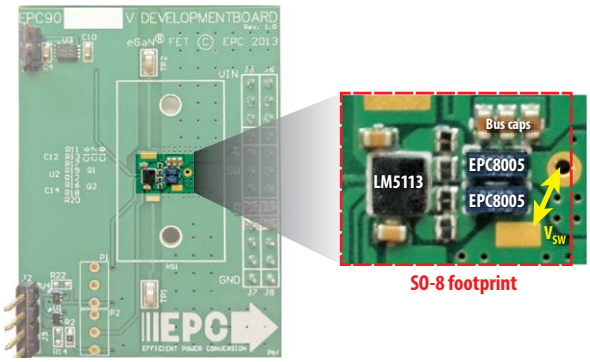

Figure 8: Photo of the evaluation board showing the EPC8000 devices and LM5113 gate driver

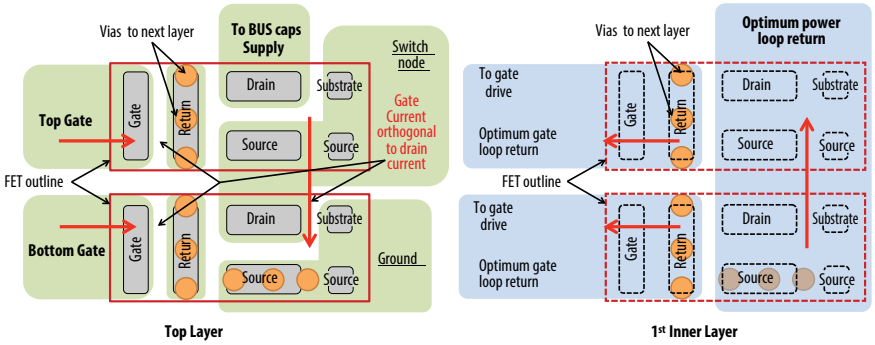

Figure 9: Optimal layout design for a half bridge topology using the EPC8000 series family of FETs. Left is the top (component) layer and right is the first inner layer.

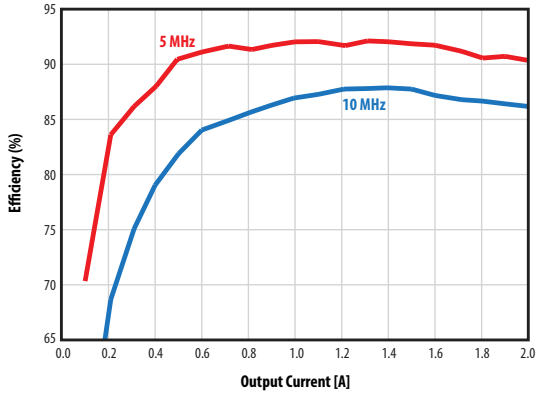

Figure 10: Efficiency plots for 5 MHz and 10 MHz operation of the envelope tracking converter

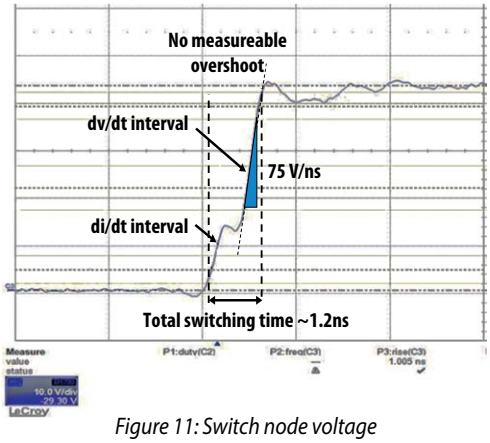

Figure 11: Switch node voltage waveform for the envelope tracker converter

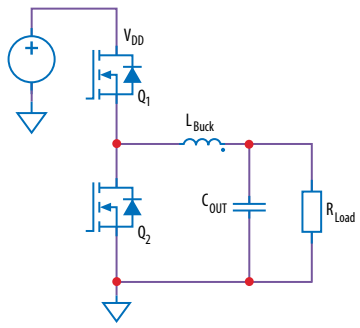

Figure 7: Envelope tracker buck converter schematic

Figure 9 shows the PCB design layout using the optimal layout technique. The left design is for the component layer (top). Note how the gate circuit currents are orthogonal to the drain circuit currents. On the right is the first inner layer design and is primarily used for the current return paths. Also note that the return paths are in the same location between the two layers where the currents flow in opposite directions, thereby cancelling the magnetic flux and hence reducing the value of parasitic inductances in the respective circuit paths.

The converter was tested at both 10 MHz and 5 MHz operation, and the efficiency is given in Figure 10. The plots show a respectable 87% peak efficiency while operating at 10 MHz and 92% while operating at 5 MHz. The inductor used in the 5 MHz operation is the same as in the 10 MHz operation, and selecting a more optimal inductance can lead to further improvement. Figure 11 shows the rising edge switch node voltage waveform with V_{IN} = 42 V, I_{OUT} = 2 A. The total switching time is around 1.2 ns and both the di/dt and dv/dt events can be distinguished. Also of note is the minimal voltage overshoot at completion of the transition.

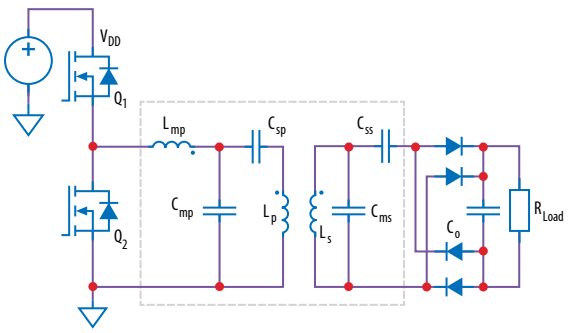

Figure 12: Voltage mode class D wireless power transfer power converter schematic

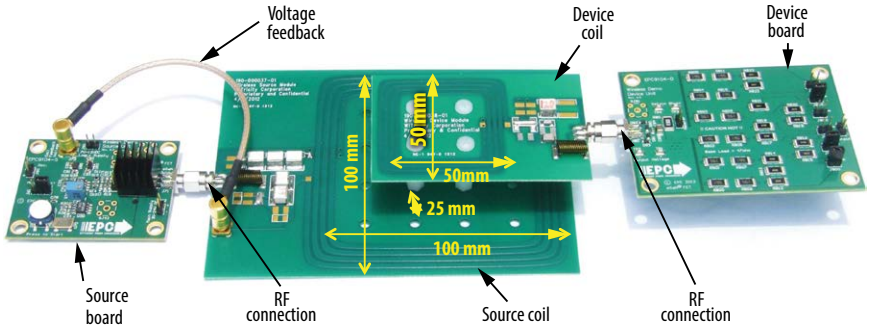

Figure 13: Photo of the wireless transfer system experimental setup

Design Example: 6.78 MHz Voltage Mode Class D Wireless Power Transfer

In the next example, a 6.78 MHz voltage mode class D wireless power transfer converter is given. This system was previously demonstrated using the EPC2014 [11, 12] and it was noted at the time that the EPC2014 was the smallest device available for this demonstration, and that the performance could improve given the correct size selection of the FETs. In this example the same coil and load set were used, and only the power converter stage was replaced with an EPC9024 populated with the EPC8004 devices. Figure 12 gives the basic schematic of the power stage.

Figure 13 shows a photo of the wireless power transfer system. The setup comprises the source board, source coil, device coil, and device load. The EPC8004 FETs were mounted to the EPC9024 board (shown in Figure 8), and the gating signals were generated from the voltage feedback control signal using a phase follower controller.

The EPC8004 based wireless system was tested by varying the input supply voltage from 8 V through 24 V, and the efficiency is shown in Figure 14. Overall there is at least a 2% increase in efficiency over the EPC2014 based version despite the higher $R_{DS(on)}$ of the EPC8004 (125 mΩ) in comparison to the EPC2014 (16 mΩ). This is mainly due to a reduction in losses associated with C_{GD} (turn off). As mentioned before, the wireless system showed reduced losses by using a smaller FET. From Figure 14 one can see that the efficiency has peaked at the high end and that the efficiency of the EPC2014 based system could potentially increase further. Figure 15 gives the loss breakdown of the wireless system when operating at 15 W load with a 22 V input. The EPC2014 has high switching losses while the EPC8004 has high conduction losses, but overall the total losses are lower than the EPC2014 for the same operating condition.

Figure 16 shows the rising edge of the switch node waveforms for both the EPC8004 and EPC2014 based converters. The measurements show that the EPC8004 solution switches much faster, which can be attributed to the many new key features of the EPC8004 device coupled with the optimal layout technique.

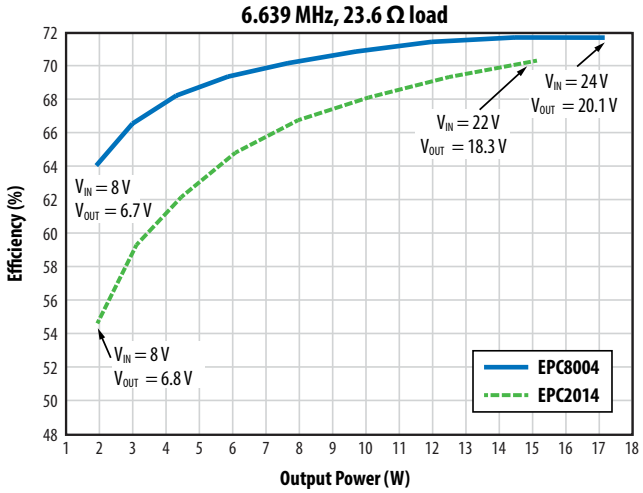

Figure 14: Wireless converter efficiency plots when using the EPC8004 and EPC2014 FETs

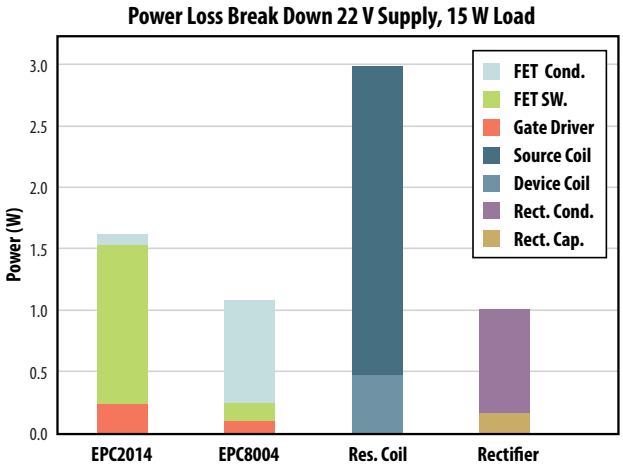

Figure 15: Loss breakdown in the wireless energy transfer system comparing the EPC8004 with the EPC2014.

Small Signal RF Performance – EPC8002

Up to this point, the high switching frequency performance of the EPC8000 series FETs have been presented. Due to the high blocking voltage in comparison to LDMOS FETs of similar ratings, the eGaN FETs have the ability to absorb higher levels of reflected energy when used in RF applications than comparable LDMOS devices. This has prompted EPC to test the eGaN FETs as RF devices and has published the results for the EPC2012 eGaN FET [17]. In this section the EPC8002 device RF tests in the frequency range 200 MHz through 3 GHz will be presented together with how this was done and how to apply the devices in RF applications.

Due to their small size and non-traditional RF package, the EPC8000 series FETs require a PCB design using tapers to connect the gate and drain circuits. The design used to evaluate the EPC8002 device is shown in Figure 17, and comprises a taper design to connect to a known transmission line impedance. In this case the substrate used was Rogers 4350 [18] with thickness of 30 mils chosen for its low losses at high frequency. Since any design using the EPC8002 devices would need this taper to connect, all subsequent data will be given up to the reference planes as shown in Figure 17.

The EPC8002 was mounted to an RF test fixture shown in Figure 18 where the design made use of 50 Ω micro-strip transmission lines to connect the gate and drain to the RF connectors, made by South West Microwave SMA [19]. The gate and drain bias was then supplied using bias Tee's from Aeroflex [20] chosen for their pulse capability rating. A heatsink was added to the top side of the device with Wakefield thermal interface material [21] to provide additional cooling to the FET. Since the EPC8002 FET is in a chipscale format and has limited thermal capability, adding a heatsink was required. However, RF bias conditions would still exceed the thermal capability limits of the FET, and as such, testing was conducted in pulsing mode with 220 µs on-time and repetition rate of 10 Hz. This effectively reduced the average power dissipation to below 500 mW and further provided sufficient time for the instruments to capture the data.

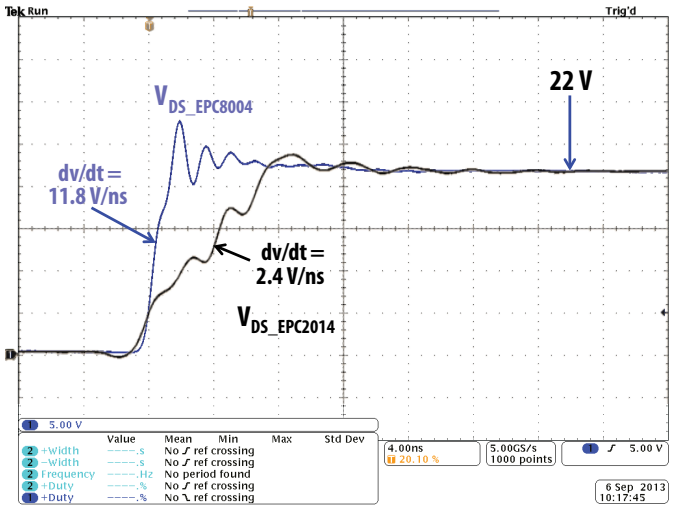

Figure 16: Rising edge switch node voltage waveforms of the EPC8004 (blue) and EPC2014 (black) based wireless converters.

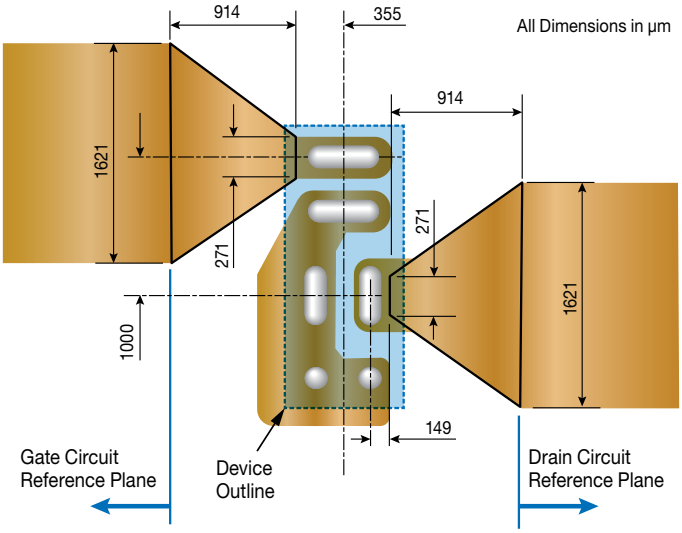

Figure 17: EPC8002 PCB design with tapers to connect the gate and drain circuits.

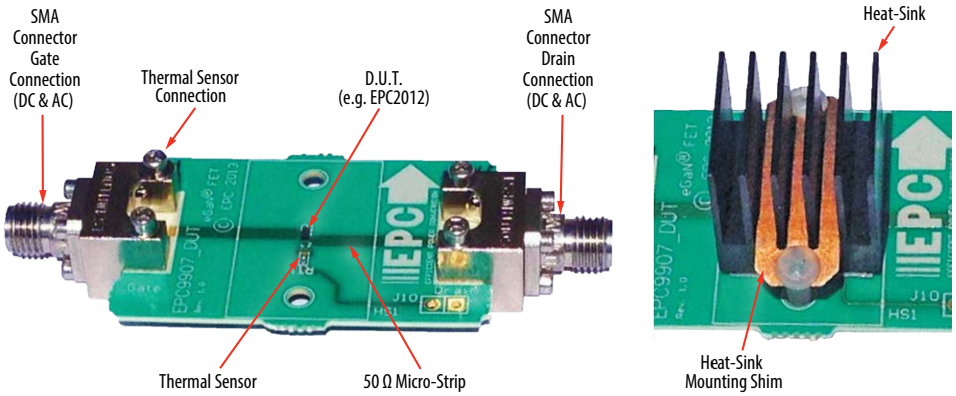

Figure 18: Photograph of the small signal RF test fixture for the EPC8002 (with the heatsink mounted shown in right image).

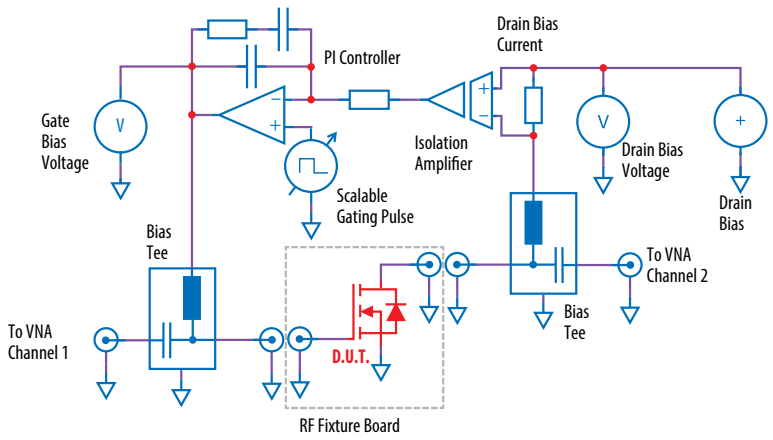

Figure 19: Basic test fixture schematic for pulsed small signal RF S-parameter measurement.

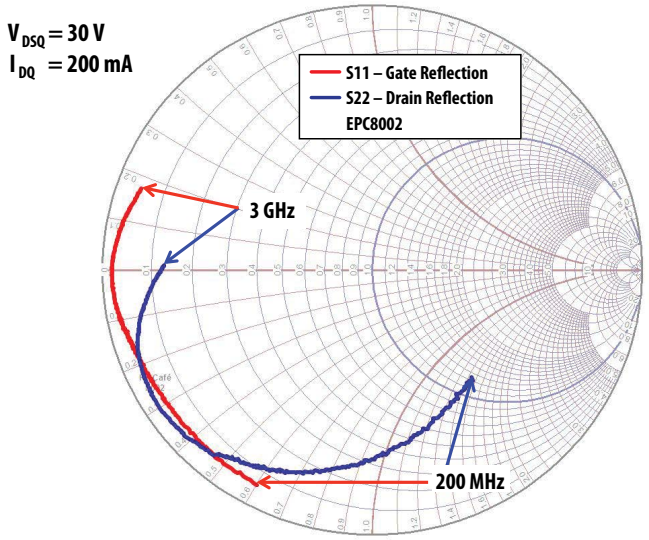

Figure 20: S-parameter plot of the EPC8002 in the frequency range 200 MHz through 3 GHz.

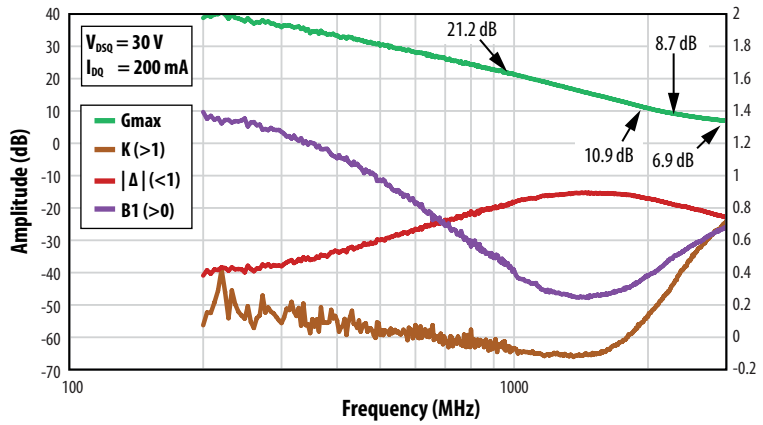

Figure 21: Max. Gain plot for the EPC8002 together with the stability markers

A special controller was developed to control the gate voltage during the on time of the pulse that measured the drain current and regulated the gate voltage to maintain the drain current to a set value. A block diagram of the pulse controller is shown in Figure 19. The custom controller was required to maintain stability of the device during the on-time and ensure a slow enough turn off as to not allow the drain current to generate a voltage overshoot in the bias Tee inductor, since that inductor is unclamped. The controller would further ensure that the gate voltage would never exceed 5 V.

Prior to the S-parameter measurement of the DUT, the VNA must be calibrated. The Thru-Reflect-Line (TRL) [23] method was utilized for calibration. The calibration process followed is well documented and similar to that described in [23, 24]. For calibration purposes EPC also developed a set of calibration standards based on the RF test fixture design and were used prior to testing to calibrate the VNA.

Figure 20 presents the gate (S11) and drain (S22) reflection results on the Smith chart for the frequency range 200 MHz through 3 GHz and V_{DSQ} = 30 V, I_{DQ} = 200 mA bias. The results clearly show very stable performance over the entire frequency range.

Figure 21 shows the maximum available gain plot over the frequency range tested, and for the same bias conditions as the Smith plot. The plot shows that the EPC8002 FET has very good gain over the entire frequency range. Also shown in Figure 21 are the stability markers, and it can be seen that all the markers show conditional stability requirements due to the high gain of the EPC8002. Extra measures are required to design an amplifier using the EPC8002 for unconditional stability.

Summary

In this application note the new 3rd Generation EPC8000 series eGaN FETs have been introduced. In addition to the advancements that existing GaN transistors offer, these third generation devices have several new features that further enable designers to take full advantage of the high performance these FETs offer. These features include a reduction in Q_{GD} thereby reducing voltage transient switching losses, improved Miller ratio providing high dv/dt immunity, low inductance pads for improved connection to both gate and drain circuits, orthogonal current flow between the gate and drain circuits for enhanced CSI reduction, and a separate gate return connection also for enhanced CSI reduction.

These new FETs exhibit very high speed performance as demonstrated in a hard switching buck converter operating at 10 MHz, and a wireless power transfer system operating at 6.78 MHz where switching voltage transients were measured in the sub nano-second range.

Even though the EPC8000 family was designed as a switching FET, they also exhibited very good small signal RF performance with high gain well into the low GHz range. To assist designers in further adopting eGaN FETs into RF applications, a reference plane design was provided.

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